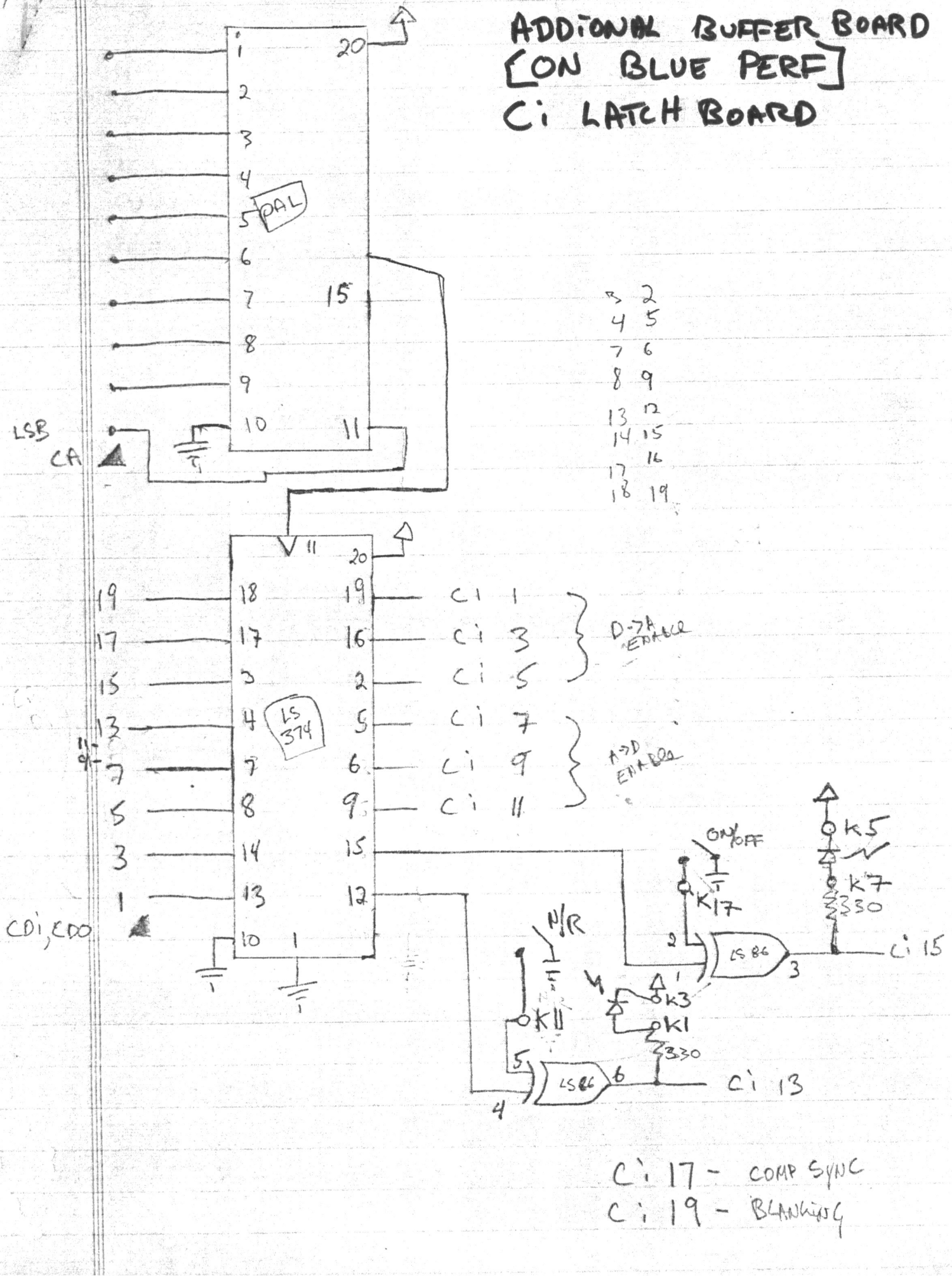
ADDITIONAL BUFFER BOARD [ON BLUE PERF]
Ci LATCH BOARD



(BUFFER)

DEAR PEER,

Ci ON A→D→A BOARD CONNECTS TO BOARD OUTLINED ON THE OTHER PAGE; AND ALSO CONNECTS TO BACK PANAL. SINCE you will USE RIBBON, THIS will be SIMPLE. ONTHE ADDITIONAL BOARD you BUILD. SPACE THE CA + [CDi/CDo] CONNECTORS THE SAME AS they ARE ON the ADDRESS BOARD FOR EASY BUSSING. THE CONNECTOR FOR THE SWITCHES & LEDS, which I CALLED K, CAN GO IN THE REMAINING SPACE. ON THE ADDITIONAL BOARD which you will BUILD, THE COMPUTER DATA IN/OUT BUS is BEING LATCHED AT A PATICULAR TIME, DETERMINED BY THE COMPUTER ADDRESS BUS DECODED BY THE PAL. This LATCHED DATA is STUFF GENERATED BY THE COMPUTER FOR Ci ON THE A/D BOARD. Ci is SPELLED OUT AT LEFT. IN ADDITION TO LATCHING you ARE ADDING EXCLUSIVE-OR GATES ON THE N/R & ON/OFF SIGNALS SO they CAN SIMULTANEOUSLY BE CONTROLED ON YOUR FRONT PANAL. This BOARD you're BUILDING ALSO NEEDS POWER SO WIRE ON IT A +5 REGULATOR AND A 8"PW" CONNECTOR. PW SHOULD BE ALIGNED THE SAME AS ON THE ADDRESS & BUFF I/O BOARDS SINCH This LATCH BOARD is GOING NEXT TO THEM.

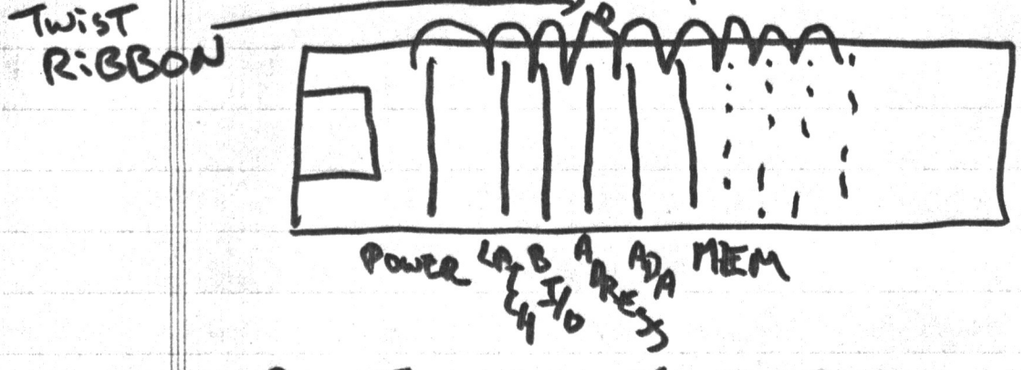
SPLIT → NOT BUSSED

Ci	
1	
3	D→A ENABLE
5	
7	
9	A→D ENABLE
11	
13	N/R
15	ON/OFF
17	COMPSYNC
19	BLANKING

DEAR PEER,

CDi AND CDO ARE NOW BEING COMBINED ON ONE BUSS SO BUSS THEM PARALLEL. They ~~are~~ ARE BRISS LABLED ADi & ADO ON ONE BOARD. The CDi/CDO THEN GOES TO YOUR GPIO BOARD IN YOUR COMPUTER ALONG with THE CA BUS WHICH WAS ALSO BUSSED PARALLEL BETWEEN THE ADD, BUF I/O & PERF, BOARDS.

* NOTICE THAT PW is REVERSED ON DIFFERENT BOARDS. IT is THE SAME ON THE ADDRESS + BUF I/O WHICH is DIFFERENT FROM THE WAY IT is ORIENTED ON THE A→D→A + MEMORY BOARDS. I BUILT THE BUFFERS with BOARDS IN THE FOLLOWING ORDER.

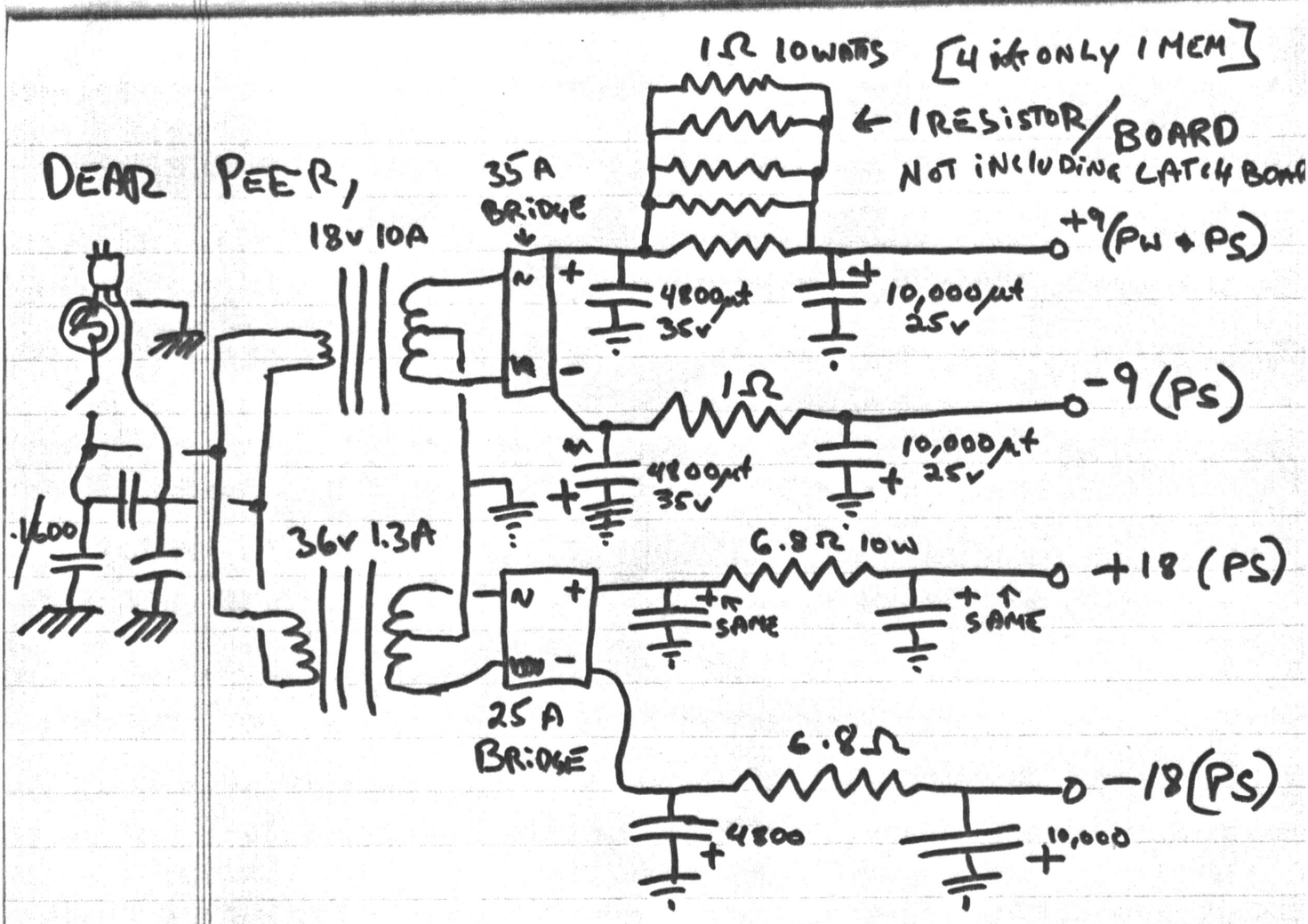


By TWISTING THE RIBBON YOU FIX ORIENTATION PROBLEM. ASK DAVE IF CONFUSED.

CK
CM } BUSS PARALLEL
*PW

ON POWER BOARD YOU WILL BUILD FOUR FILTERS. +5 GETS 5 OR six 1Ω OHM 10 WATT IN PARALLEL - LOSS OF POWER. BOTH PW + PS GET +5 FROM THIS SAME FILTER.

DEAR PEER,



PS GOES TO ADA BOARD
EX GOES BETWEEN BUFF I/O & ADDRESS

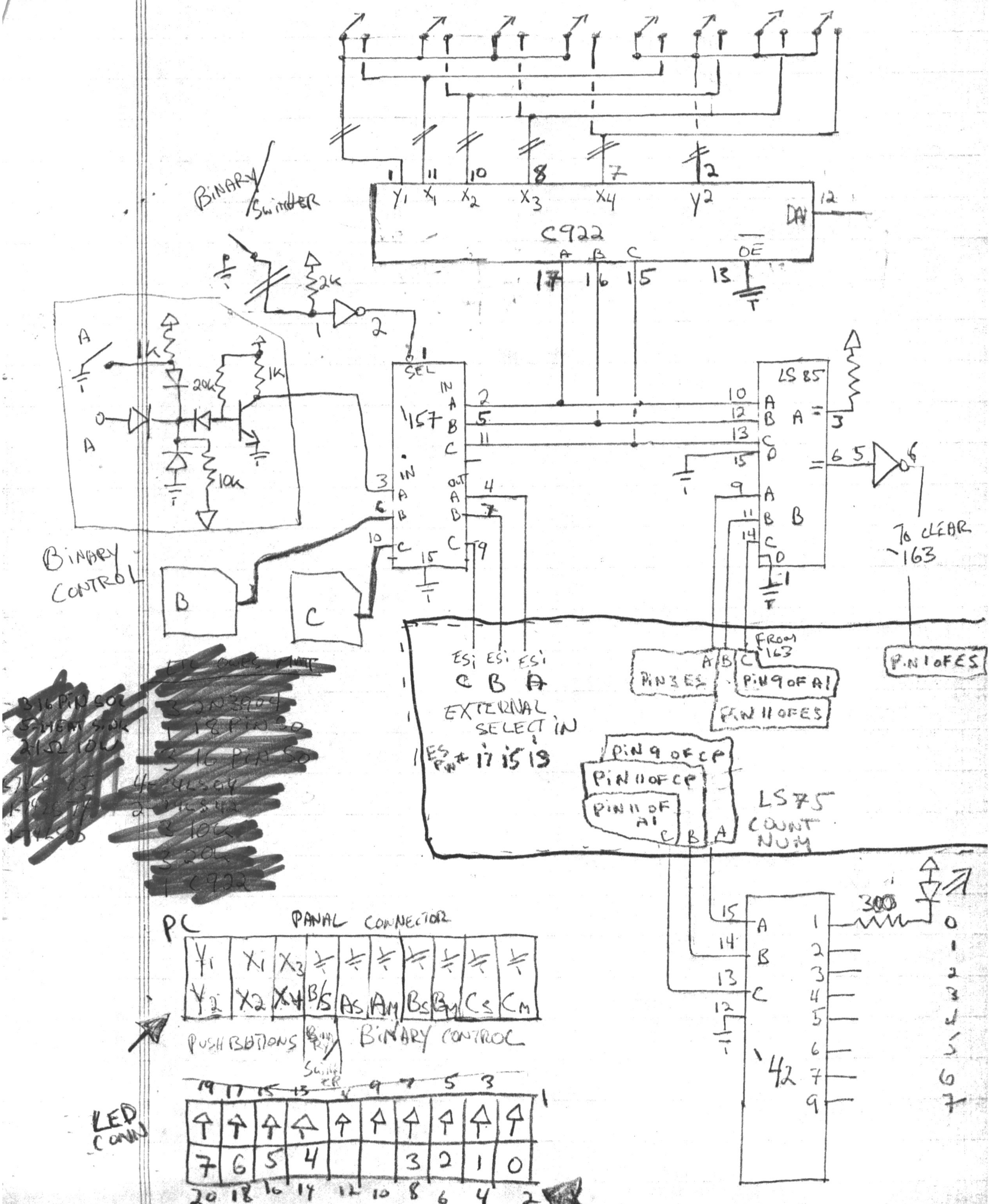
ASK DAVE FOR PHOTO STATS FOR EACH BOARD WITH PINOUTS FOR CONNECTORS IN QUESTION.
MAKE CERTAIN THERE ARE EIA → TTL CONVERTERS ON THE ADA BOARD
220pf CAP IS FOR ADDRESS BOARD - ASK DAVE WHERE

34 PIN BUSSING:
Di
DO
WR
AD
} BUSS PARALLEL

BEST WISHES

Matthew

ONLY A PHONE CALL AWAY

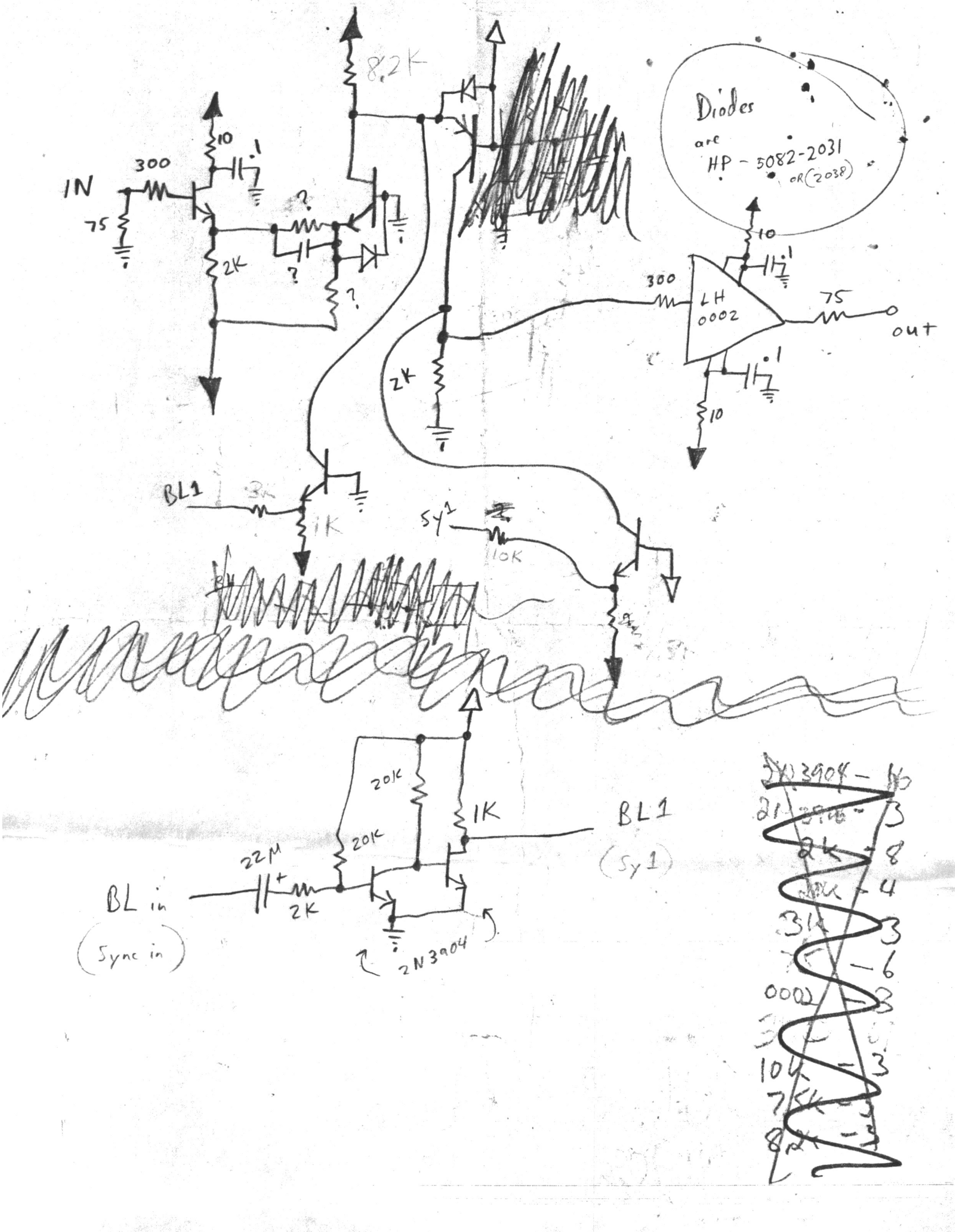


SEQ

⏚	⏚	⏚	⏚	⏚	⏚	⏚	⏚	⏚	⏚
A	B	C	CL END	A	B	C	ES 1A	ES 1B	ES 1C

COUNT NUM '163 CLEAR FROM '163 *

CARRY OUT ON ES CONNECTOR ON SEQUENCER CHANGES TO A FROM '163.


IN
300
75
10
.1
2K
8.2K
Diodes are HP - 5082-2031 or (2038)
10
.1
300
LH 0002
75
out
.1
10
2K
BL1
3K
1K
Sy1
10K
20K
20K
1K
BL1
(Sy1)
22M
+
2K
BL in
(Sync in)
2N3904

SEQUENCER KEYER

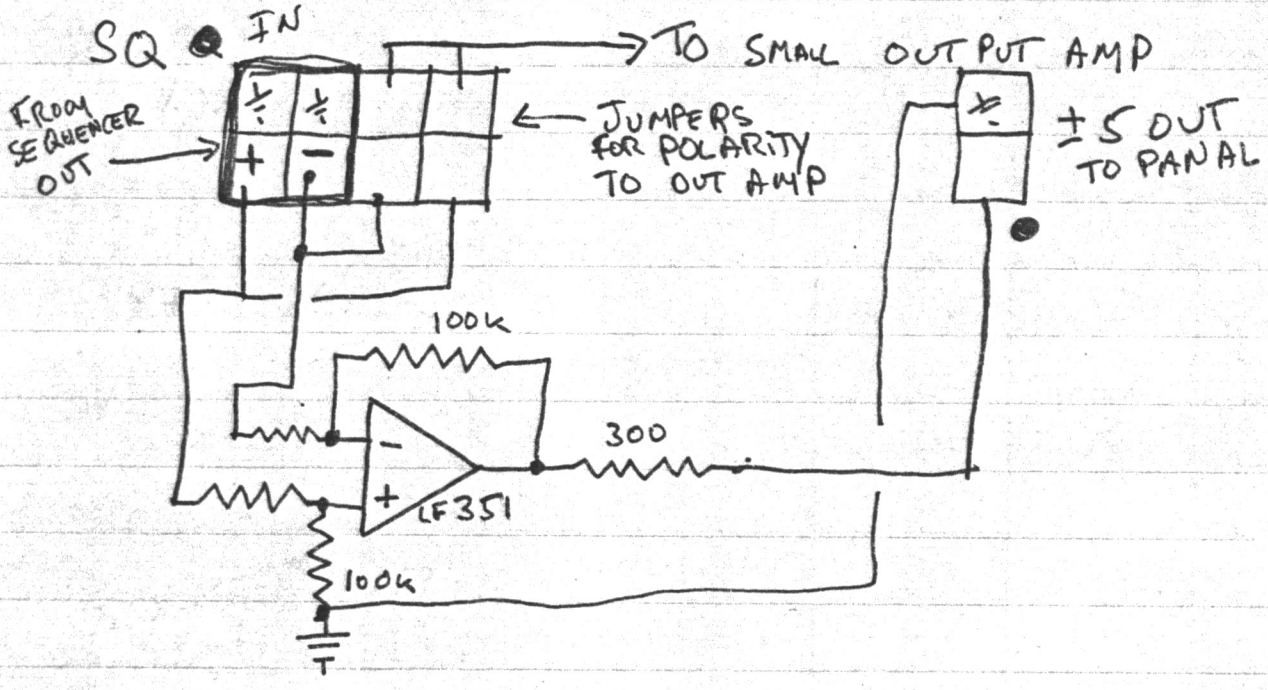
ADDITIONAL PERF BOARD #1

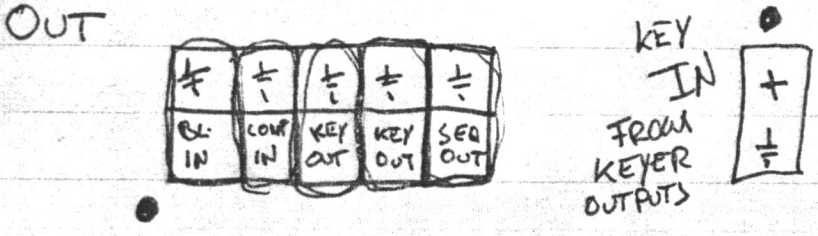
3 SMALL SYNC INSERTER OUTPUT AMPS

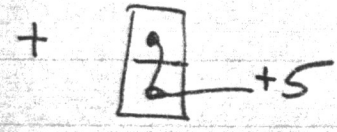
1 DIFFERENCIAL AMP FOR SEQUENCER ±5 OUT

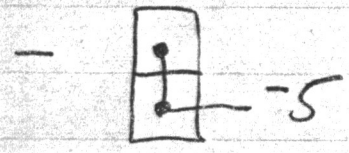
POWER REGULATION FOR FRONT PANAL

AS WELL AS BOARD









PRINTER BOARD BUFFER MODIFICATION

DAVE - SUPPLY 2 - 74LS244's

$\overline{RD}$ & $\overline{WR}$ ARE NOT WIRED I DID NOT KNOW WHERE TO.

FOR BUFF { $\overline{RD}$ is AT PIN 6 OF LS32
$\overline{WR}$ is AT PIN 8 OF LS32

? WAS NOT SURE - ADDRESS A_0 is $\emptyset$ ON BUFF BUSS

S-100

A0	–	79
A1	–	80
A2	–	81
A3	–	31

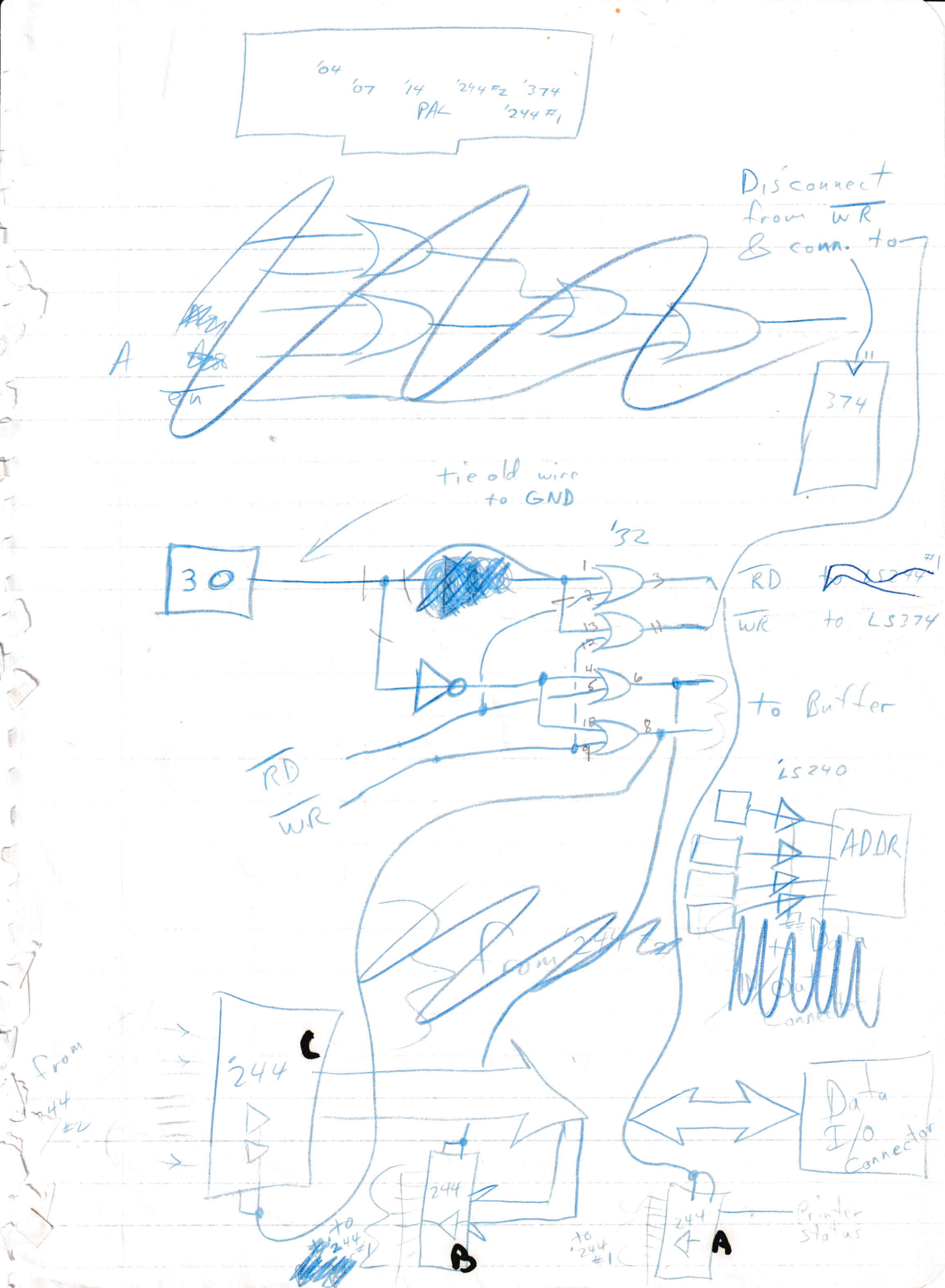
DO 0	–	36
1	–	35
2	–	88
3	–	89
4	–	38
5	–	39
6	–	40
7	–	~~30~~ 90

DI 0	–	95
1	–	94
2	–	41
3	–	42
4	–	91
5	–	92
6	–	93
7	–	43

244 # D		ADDRESS
2	18	0
4	16	1
6	14	2
8	12	3

244 # 2		244 # C		I/O
2	18	2	18	0
4	16	4	16	1
6	14	6	14	2
8	12	8	12	3
11	9	11	9	4
13	7	13	7	5
15	5	15	5	6
17	3	17	3	7

74LS244 # 1		74LS244 # B		I/O
18	2	18	2	0
16	4	16	4	1
14	6	14	6	2
12	8	12	8	3
9	11	9	11	4
7	13	7	13	5
5	15	5	15	6
3	17	3	17	7


'64
'07
'14
'244 #2
'374
PAL
'244 #1
Disconnect from WR & conn. to
A
374
tie old wire to GND
30
'32
RD
WR
to Buffer
'LS240
ADDR
'244
C
B
A
Data I/O Connector
Printer Status

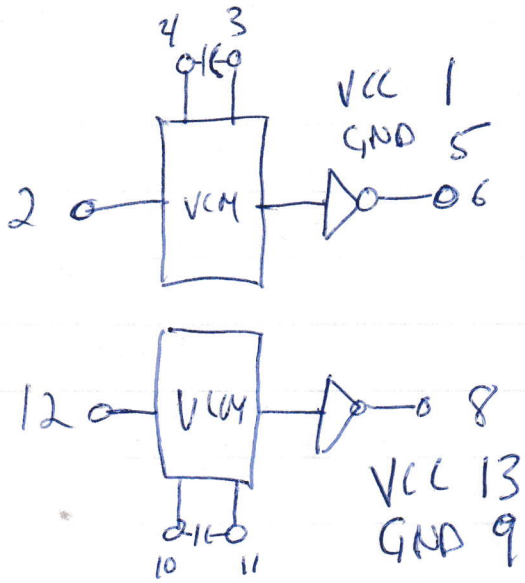
(1) Add 2 'LS244's with outputs tied together and going to the inputs of LS244 #1

what is now going in to pin 2 of 'LS244 #1 will now go to pin 2 of one of the New LS244's. the other '244 gets its inputs from the Data I/O connector

(2) a third New '244 gets its inputs from '244 #2 outputs. the outputs of the 3RD New one go to the Data I/O connector

(3)

4024 100µf & .1µf



OUTPUT POWER
14 VCC
7 GND